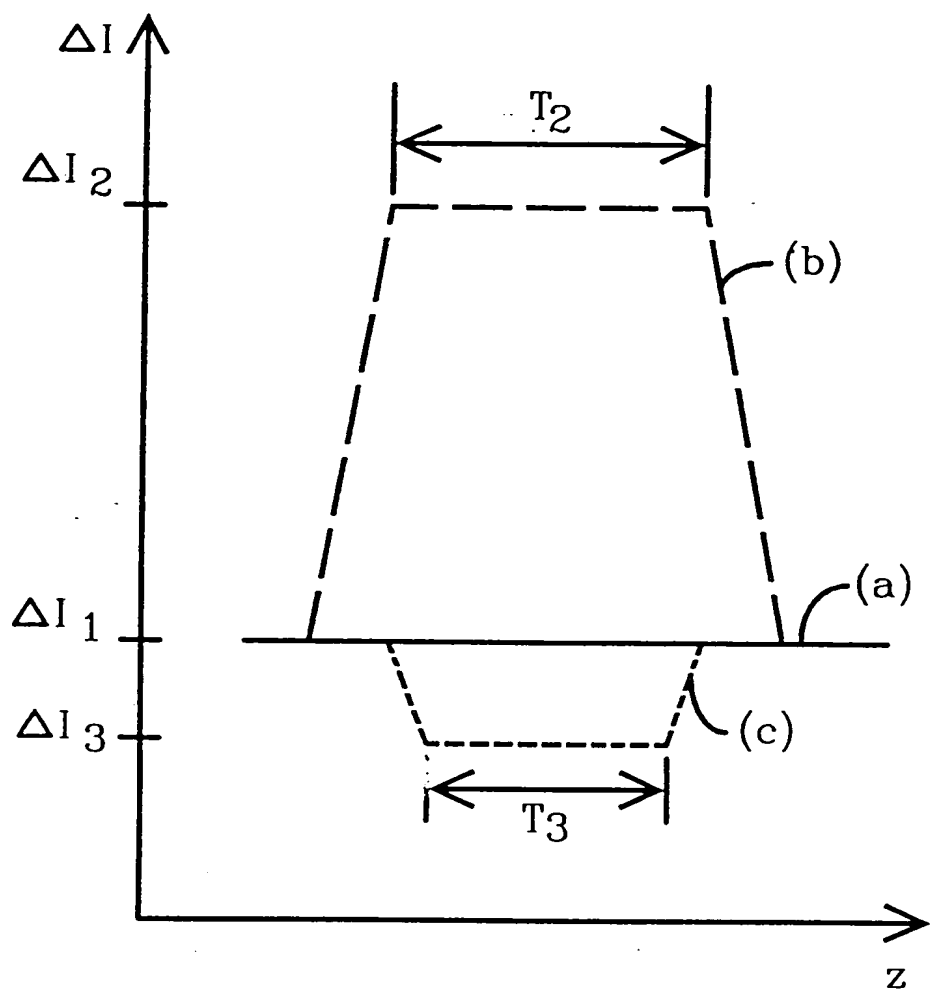


FIG. 1



PRIOR ART

FIG. 2

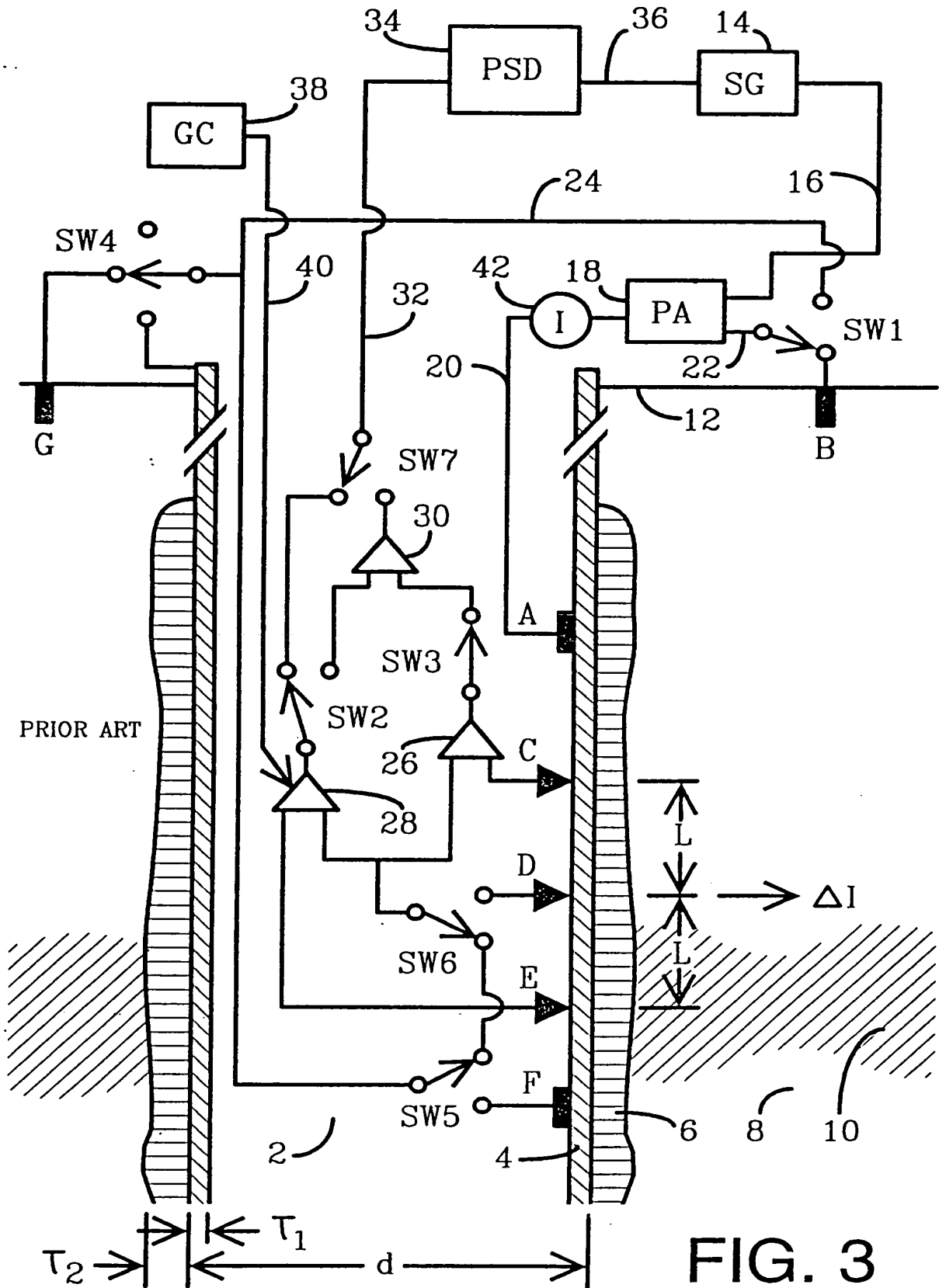
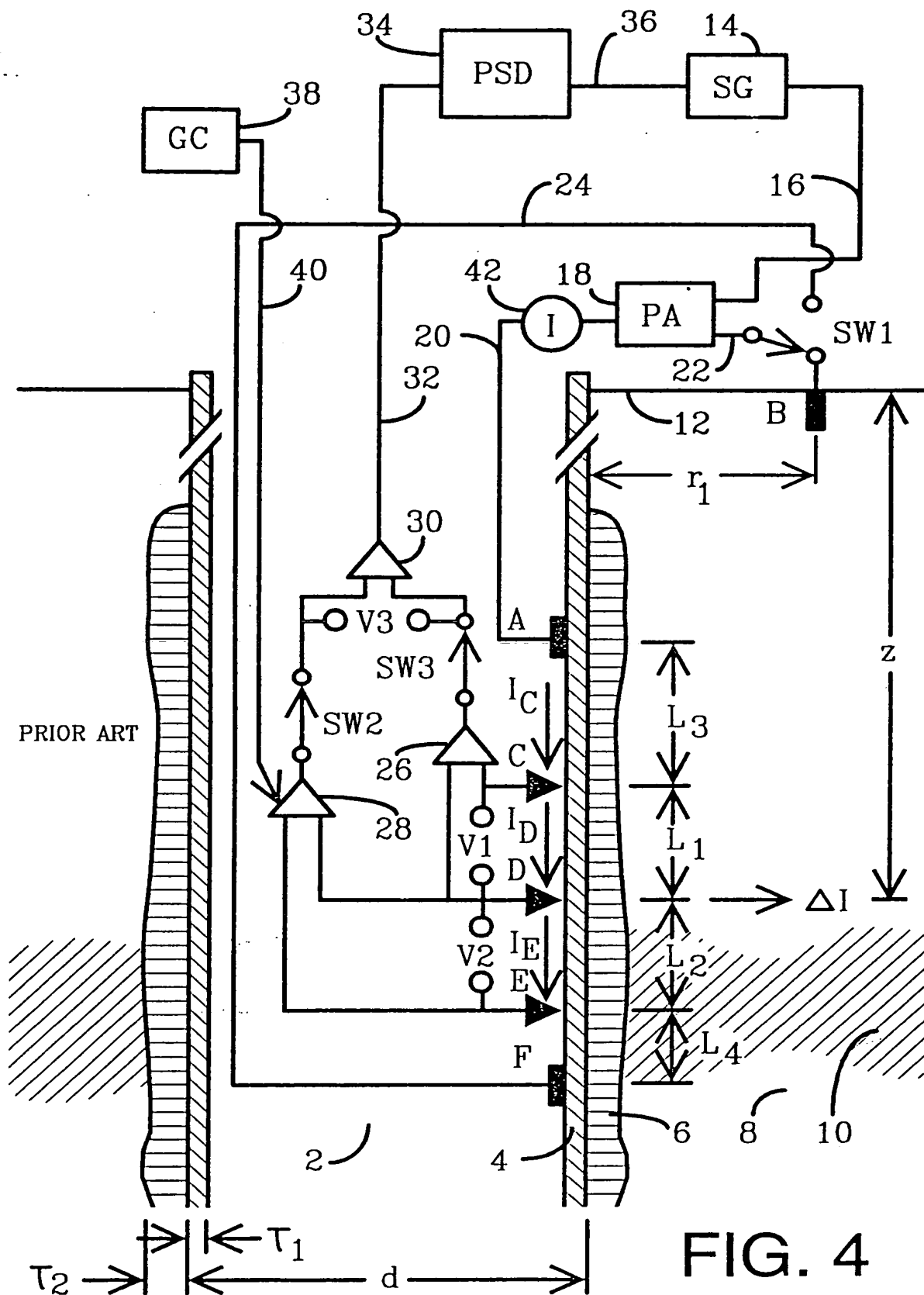


FIG. 3



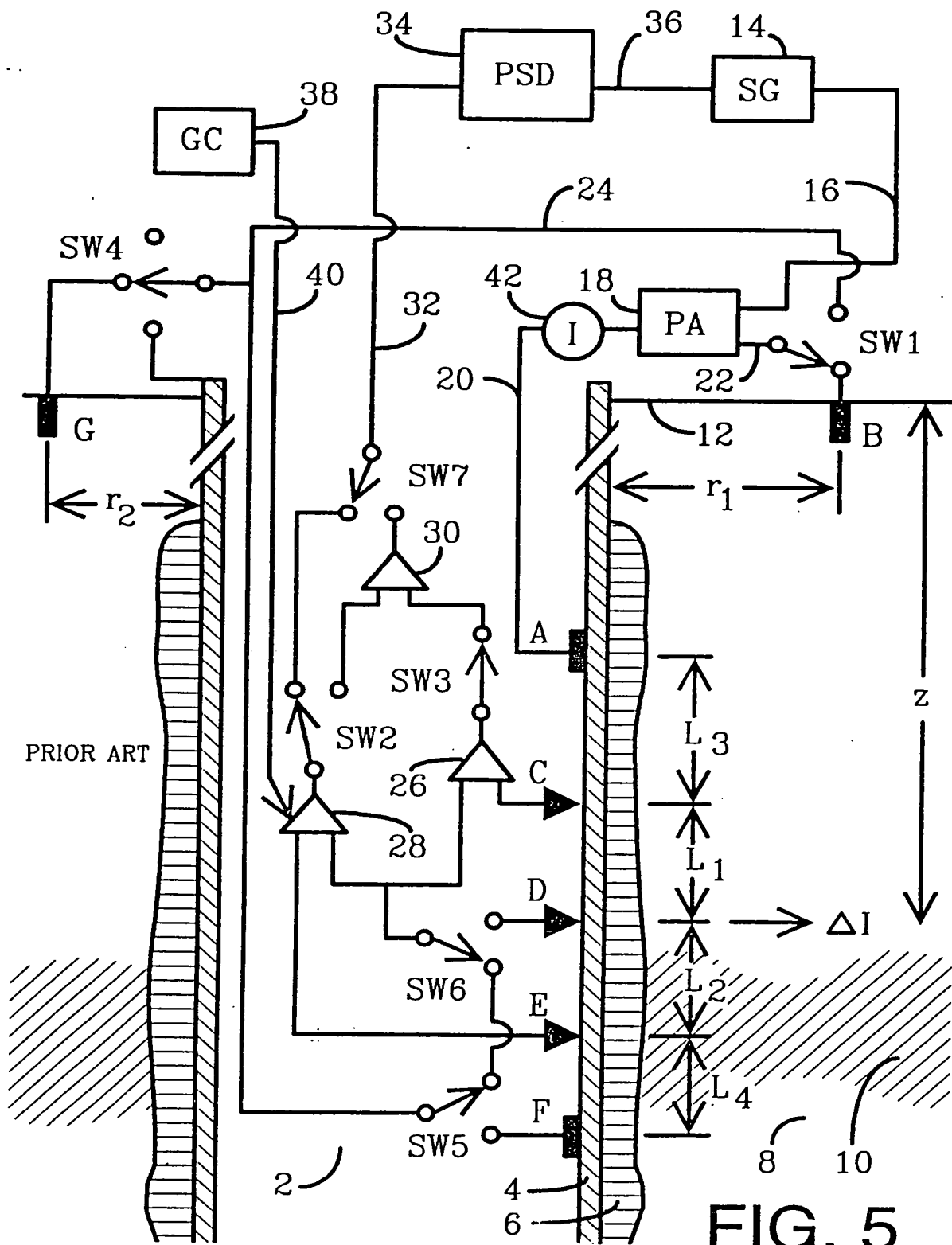
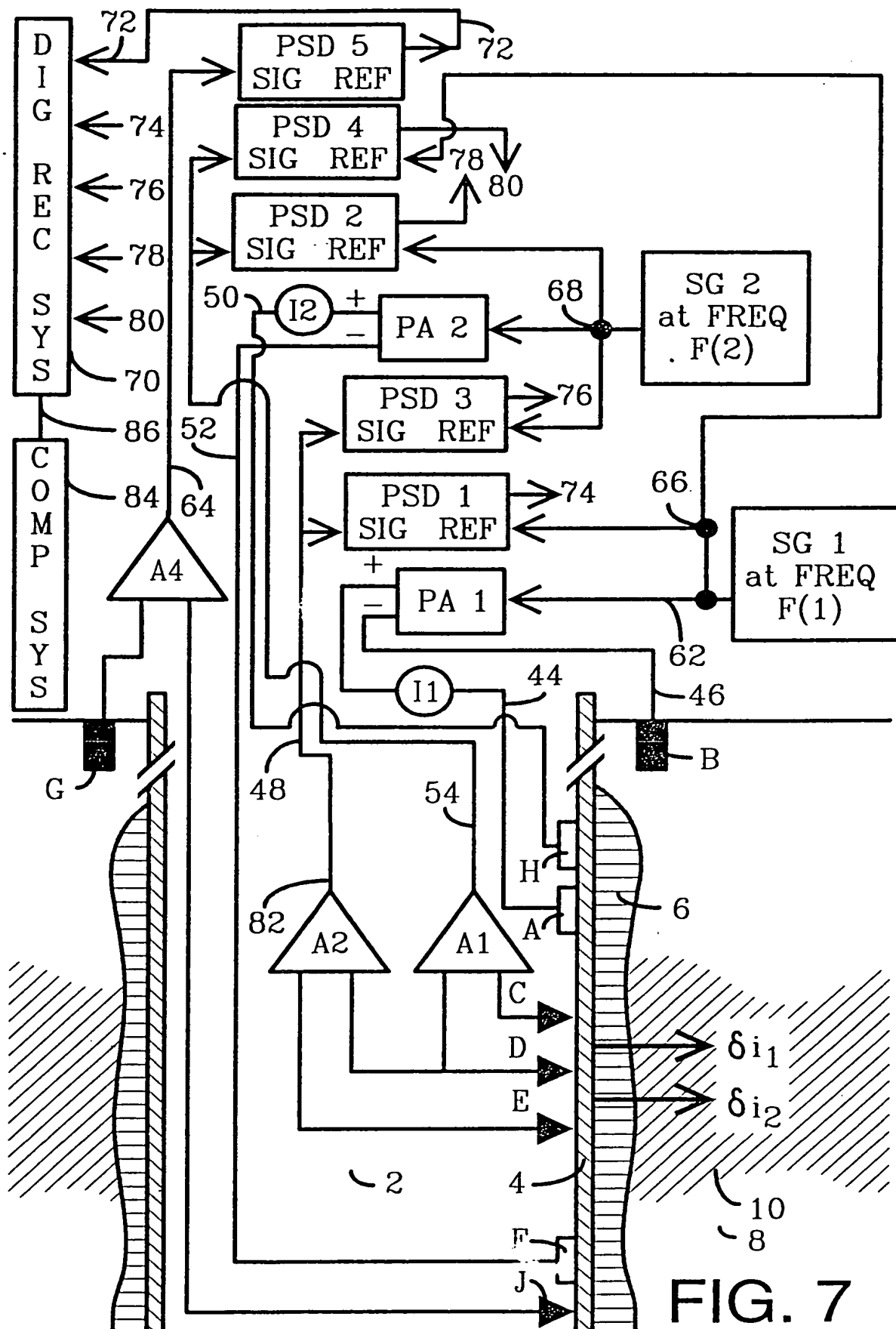


FIG. 6 is a block diagram of a closed-loop system for a variable capacitor. The system includes a digital recording system (DIG REC SYS) and a compensation system (COMP SYS). The digital recording system outputs signals 72, 74, 76, 78, and 80 to various components. The compensation system includes a summing junction (A4) and a feedback loop. The feedback loop consists of a series of PSD blocks (PSD 5, PSD 4, PSD 2, PSD 3, PSD 1) and PA blocks (PA 2, PA 1). The PSD blocks are labeled "SIG REF". The PA blocks are labeled "PA 2" and "PA 1". The system is driven by two signal generators: "SG 2 at FREQ F(2)" and "SG 1 at FREQ F(1)". The output of the system is a variable capacitor (6) with terminals A, B, C, D, E, F, H, and J. The capacitor is shown in cross-section with a dielectric material (8) and a conductive layer (10). The system is labeled "PRIOR ART".

FIG. 6



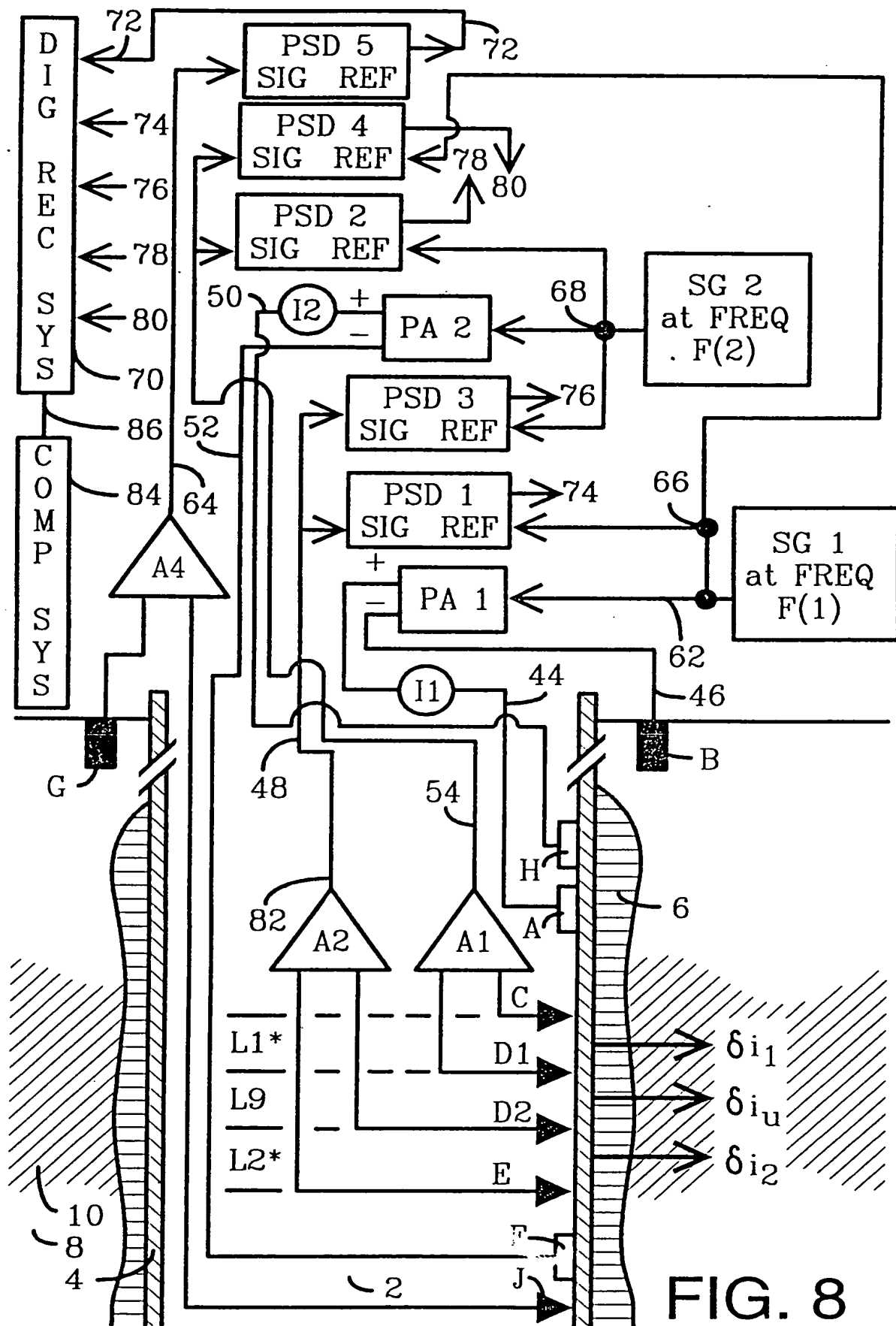


FIG. 8



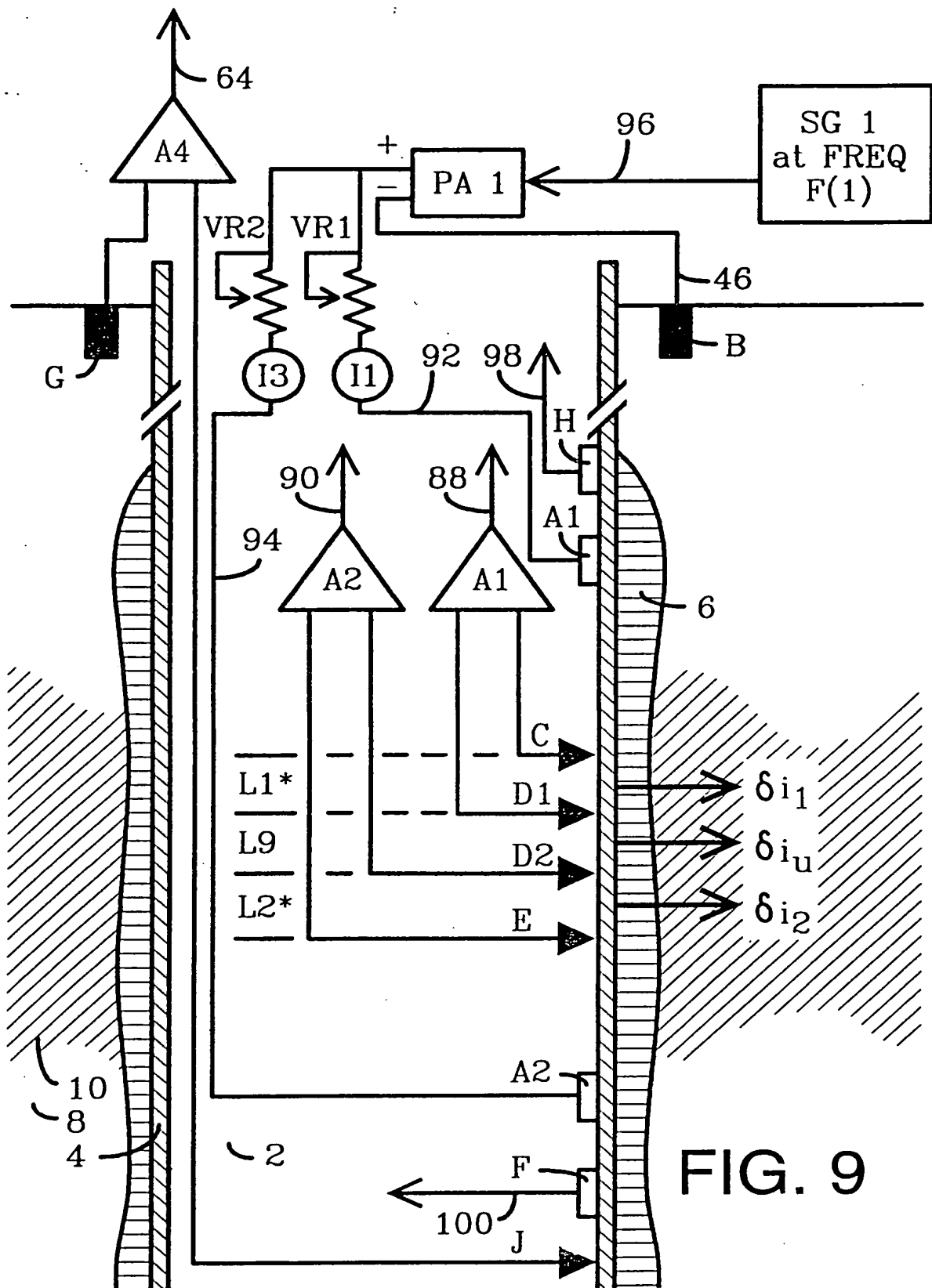
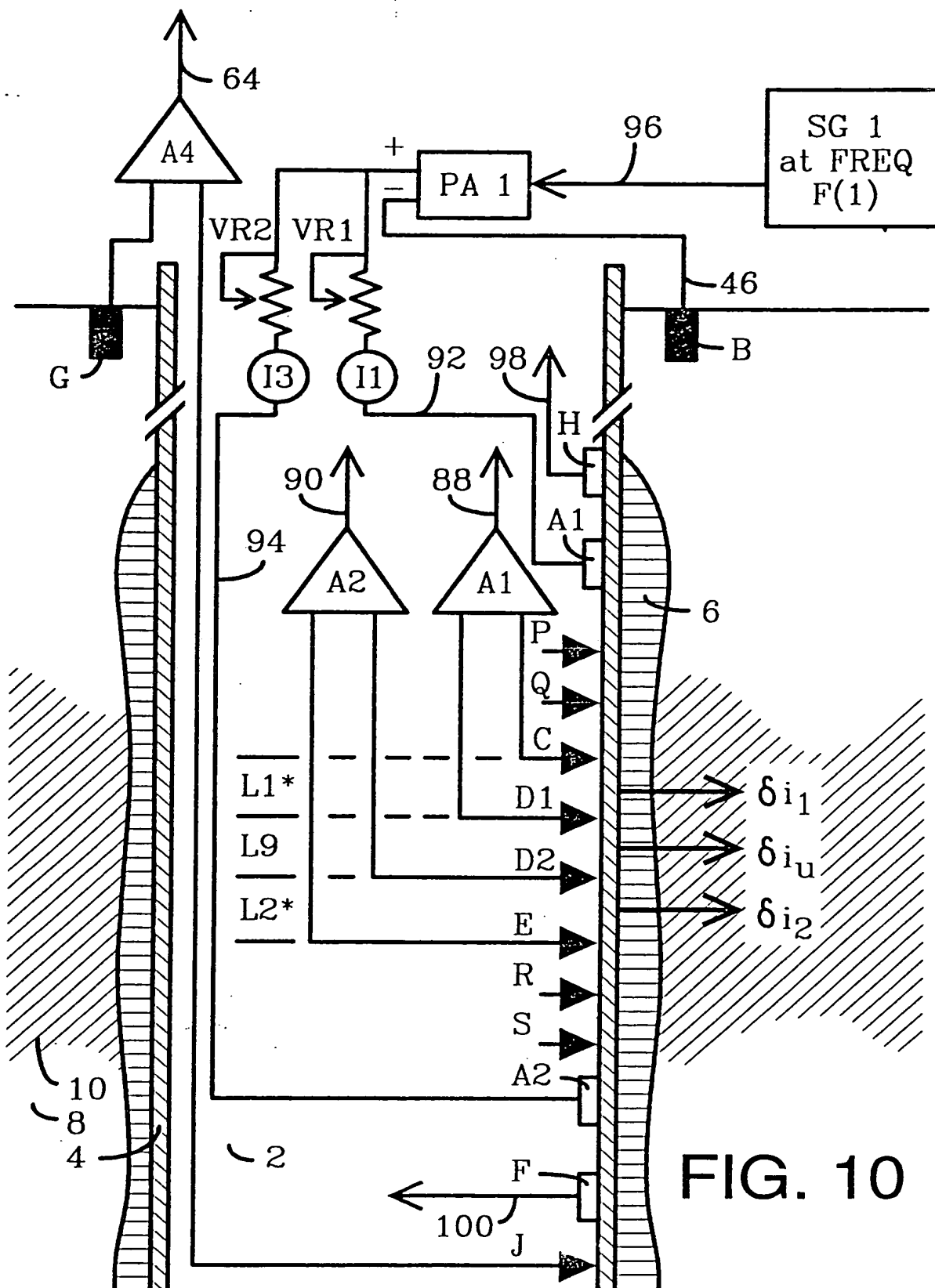
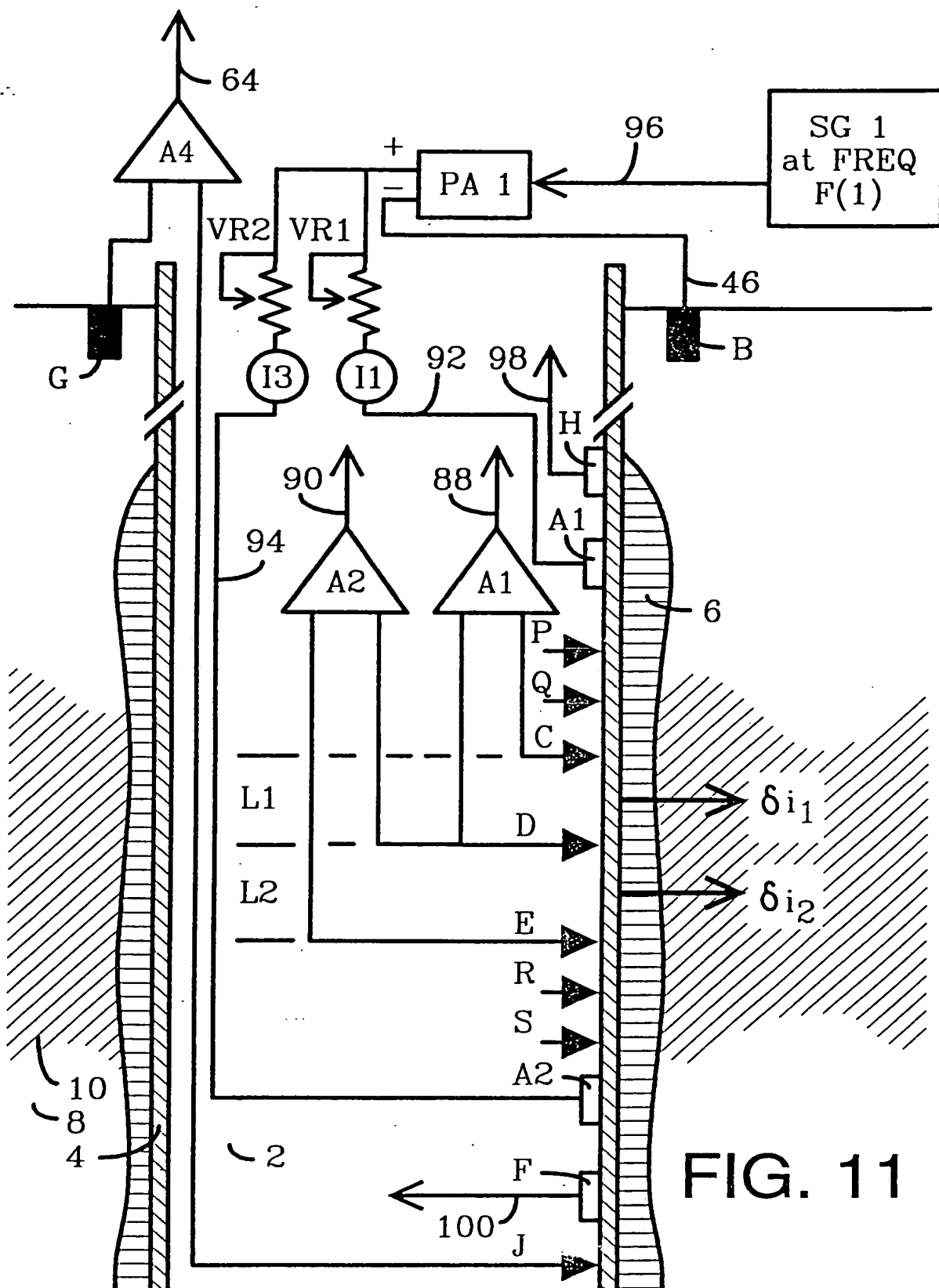


FIG. 9





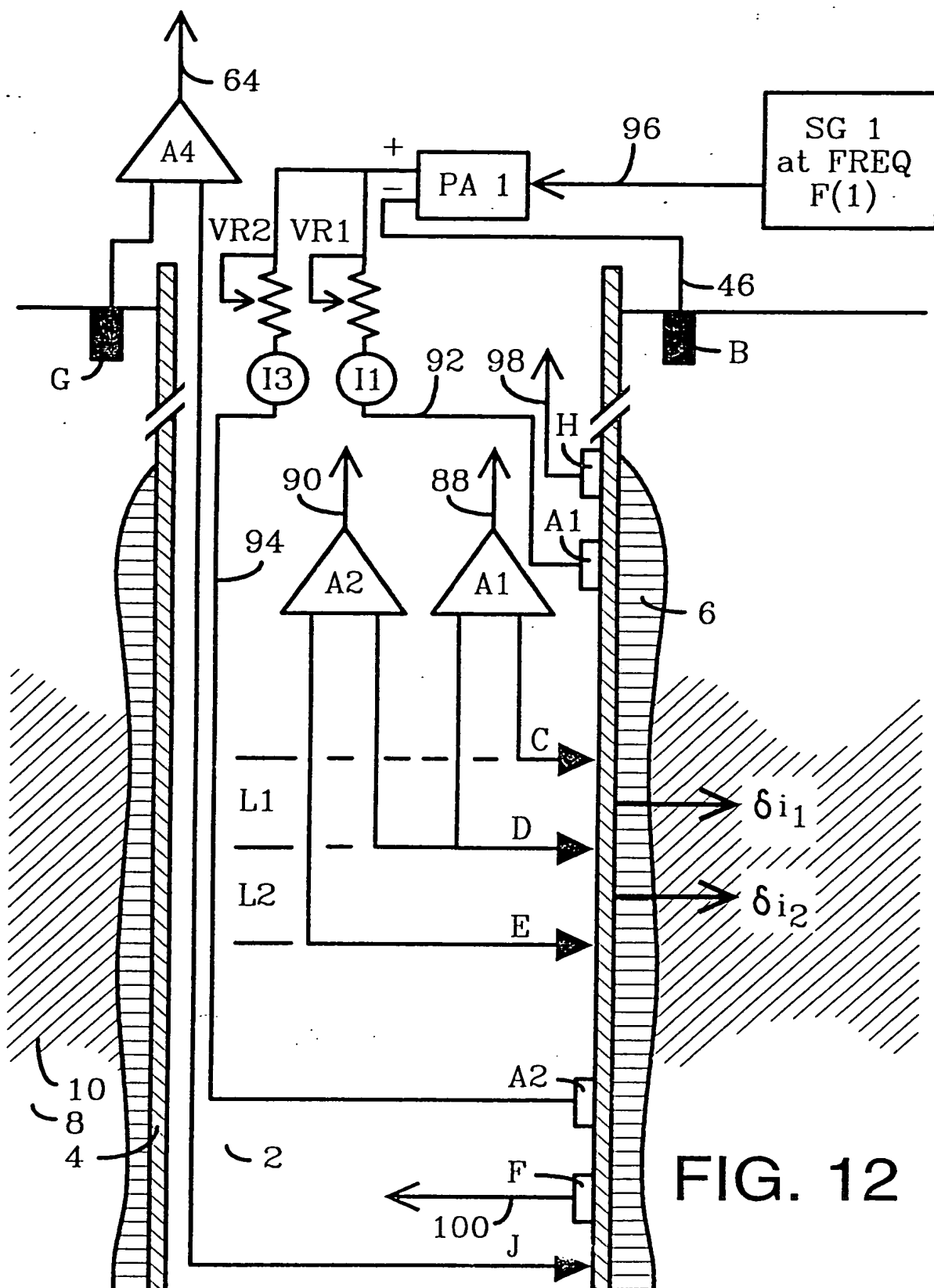


FIG. 12

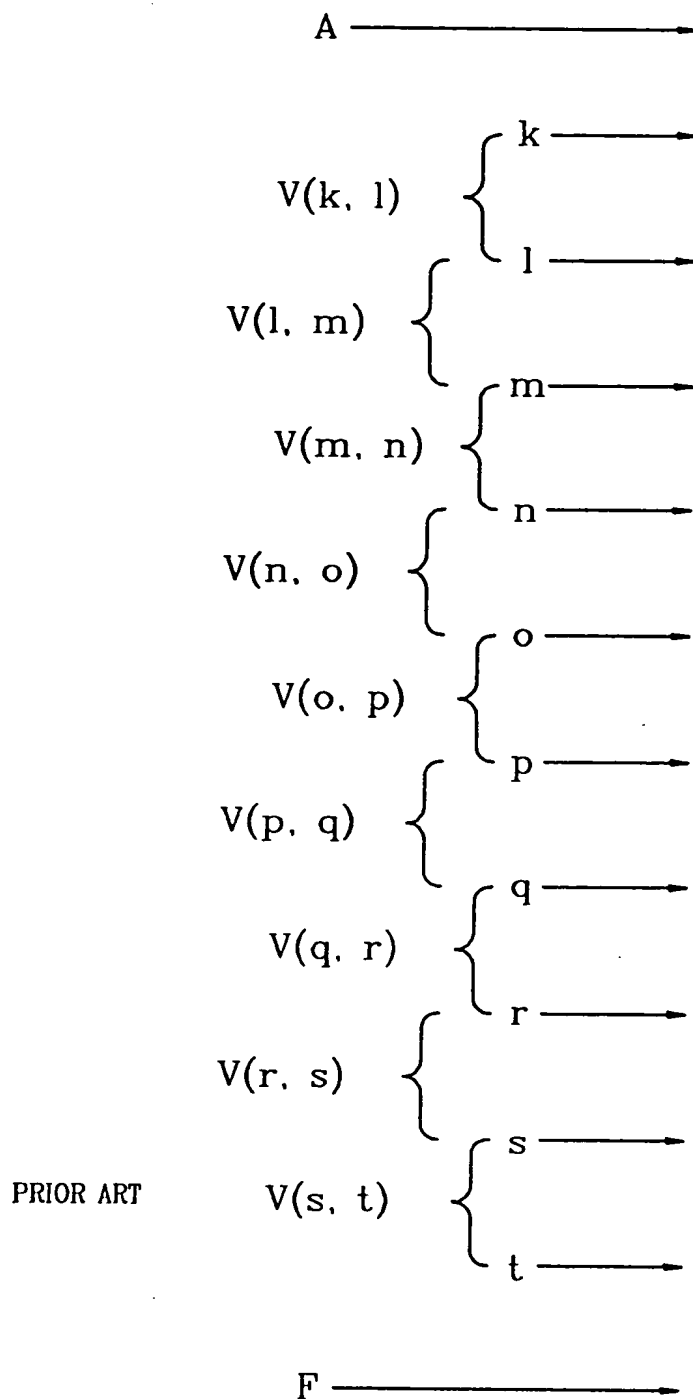


FIG. 13

